TDT4295 Computer Design Project

Assignment Text

2014

The performance increase available from harvesting Instruction Level Parallelism (ILP) from the serial instruction stream is limited because we have reached the maximum power consumption that can be handled without expensive cooling solutions [1]. Energy efficiency is now a primary metric for optimization across all kinds of computers. As such, architectures that depart from the traditional aggressive out-of-order superscalar processor pipeline and exploit parallelism in different ways are increasing in importance.

This year the group has to make a decision on what kind of processor you would like to make. We are open for two different types of processors:

Option 1: Construct an asymmetric multicore processor.

Asymmetric multicore processors [8] combine high performance and power efficient cores on a single chip. A recent implementation example is ARM's big.LITTLE [7] concept. By combining one or more high performance cores with one or more cores optimized for power efficiency, this approach aims at lowering the average energy consumption of the system. This is accomplished by mapping different applications (or different parts of the same application) to the big/small cores.

Option 2: Construct a graphics processing unit (GPU) inspired processor.

GPUs play a large role in graphical applications as well as high performance computing. They are typically constructed around the SIMD (single instruction multiple data) paradigm and include special hardware for accelerating graphics-related operations. The idea is to make a GPU-inspired processor architecture that exploits the possibility of parallel computation on a single chip. The GPU must (as in option 1) be a multi-core system.

Additional requirements

Your processor will be implemented on an FPGA, and you are free to choose how to realize your computer architecture. Studying the architecture of general multi-core processors [6], and parallel machines options [2, 3, 4, 5] can be a good starting point.

Energy efficiency should be a primary consideration in all phases of the project, from early design decisions to how software is written.

The task should also include a suitable application that can produce a graphical output on a display to demonstrate the processor.

The unit must utilize a Silicon Labs EFM32 series microcontroller (to act as an I/O processor)

and a Xilinx FPGA (to implement your architecture on). The budget is 10.000 NOK, which must cover components and PCB production. The unit design must adhere to the limits set by the course staff at any given time. Deadlines are given in a separate time schedule.

And a final tip; ***Keep it simple, as simple as possible, but not simpler.***

Evaluation

The project is evaluated based on the project report and an oral presentation of the work as well as a prototype demonstration. One grade will be given to the group as a whole, unless there are significant variations in the amount of effort put into the project.

References

1. Borkar and Chien; The Future of Microprocessors; Communications of the ACM; 2011
2. Bell et al.; TILE64 - Processor: A 64-Core SoC with Mesh Interconnect; ISSCC; 2008
3. Kongetira et al.; Niagara: A 32-way Multithreaded SPARC Processor; IEEE MICRO; 2005
4. Wikipedia; Goodyear MPP; http://en.wikipedia.org/wiki/Goodyear_MPP
5. M Flynn; Some Computer Organizations and Their Effectiveness; IEEE Transactions on Computers. Volume:C-21 , Issue: 9. 1972
6. Wikipedia; Multi-core processor; http://en.wikipedia.org/wiki/Multi-core
7. big.LITTLE Processing; http://www.arm.com/products/processors/technologies/biglittleprocessing.php
8. Fedorova, Alexandra, et al. "Maximizing power efficiency with asymmetric multicore systems." Communications of the ACM 52.12 (2009): 48-57.