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The What, Why, and How of MPSoCs

Chap. 1 in *Multiprocessor Systems-on-Chips,*
Ahmed Amine Jerraya & Wayne Wolf, Elsevier, 2005.

1. What are MPSoCs ?
2. Why MPSoCs ?
3. Challenges
4. Design Methodologies
5. Hardware Architecture
6. Software

MPSoC

- Multiprocessor systems-on-chip
  - Made possible by VLSI technology
    - 100 – 1000 million transistors/chip
  - ***"Harnessing all this raw computing power requires designers to move beyond logic design into computing architecture"***
- Systems-on-chip (SoC)
  - "Is an integrated circuit that implements most or all of the functions of a complete electronic system"
  - Keywords:
    - Complexity, analog & mixed signal IO, specialized HW, custom architecture (→ heterogeneous MP when MP)
- Most SoCs are MPSoCs
  - Easier to guarantee real-time performance

SoC product categories

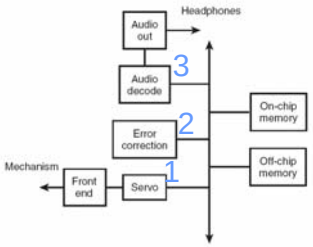
- Cell phones, PDA's, Digital Camera, MP3player etc.…
- Telecomm/networking, network processors
- Digital television, set-top boxes
- Television production equipment: video camera etc.
- Video games
- Uniprocessor SoC sufficient for simpler applications, example PDA
- +++
- A large number of Norwegian companies in the area
  - Sensonor, Seatex, Nordic semiconductor, Atmel Norway, Falanx (now ARM), ChipCon (now TI), Energy Micro, +++

(MP)SoC benefits

- Compared to general-purpose computer architecture:
  - More cost effective
    - Consumer market requires very low prices
  - Better performance
    - …through specialised HW/SW solution
  - **"The good circle of embedded systems:"**
    - "One application" ⇒ easier to use specialised HW ⇒ easier to make integrated solution ⇒ easier to make single-chip-solution / small scale ⇒ cheaper product ⇒ more likely to have "one product pr. application"

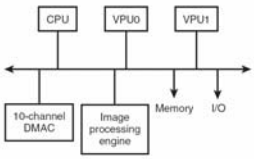
Example: CD/MP3 Player architecture

- Different processing elements (PEs)
  1. CD drive
     - Analog IO
     - Digitally controlled by a DSP
  2. Error correction
     - Special-purpose HW
  3. MP3 decoding
     - Simple CPU



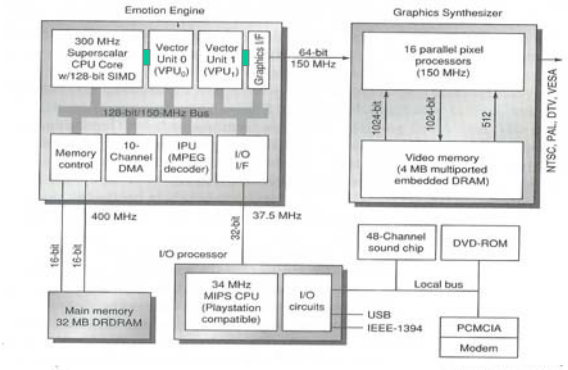
Example: Playstation 2 (PS2)

- Emotion Engine + Graphics Synthesizer + IO-processor
- Subsystems are SoCs
- Emotion Engine is MPSoC
  - See also [HP03] (course TDT4260)



PS2 Emotion Engine

PS2 – block diagram



MPSoC characteristics

- Real time performance
  - Many SoC systems require a performance guarantee
    - In contrast to average performance
- Low energy consumption
  - Battery operated
  - Small systems more difficult to cool
  - Chip packaging; plastic cheaper than ceramic
- HW/SW codesign
  - Late decision about using HW, SW or a HW/SW solution for a given component
    - Partitioning
    - HW/SW cosimulation
- Very reliable SW needed
  - Supplied as part of the chip, no extra chance to fix later

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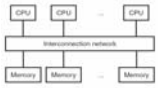
Heterogeneous MP vs. symmetric MP



- Heterogeneity
  - Different types of PEs (P)
  - Heterogeneously distributed memory (M)
  - Heterogeneous interconnection network (P <-> M)
- Heterogeneous multiprocessing
  - Harder to program, but potentially better for
    - real-time
    - area-efficiency
    - energy-efficiency
  - One more powerful processor core will reduce the effect of Amdahl's law (serial fraction putting a limit on maximum achievable speedup)
- Discussion
  - One general SMP-based platform vs. many specialised heterogeneous MPSoCs?
  - FPGA w/embedded processor as compromise?

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Benefits of special purpose HW

- Special purpose PE can be faster and smaller
  - Matching datapath width with native data size
  - Matching cache size and organization with application need
- Memory specialization
  - Matching size and organization with application
  - Example: PS2
- Reduced area ➔ reduced power

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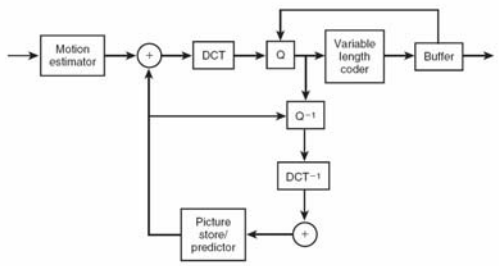
Task level parallelism often inherent in embedded computing



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Challenges

- Melding of hardware and software design disciplines
- High reliability SW
- Real time performance
  - Real-time OS, kernels (Example QNX)
- Small "memory footprint"
  - Compression (Later in this course)
- Low energy
- Modern MPSoC systems are targeted at multiple customers
  - "external" SW designer ➔ development environment needed

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More challenges

- MPSoC architecture
  - As networks-on-chip; packet networks
    - SoC applications with specific traffic patterns
      - How to exploit ?
  - FPGA as a part of SoC?
    - Where to put the FPGA?
      - How to use?, tools?
- Security
- Integration into networks of chips
  - Sensor networks
  - Examples; automotive, avionics, …

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Design methodologies & tools

- Goals
  - Short design time (time to market)
    - RTL design is too low level!
    - Higher level abstractions
  - Required performance/power/production cost
    - Predictability of results
    - Meeting design metrics
- Design components are heterogeneous
  - HW or SW
  - Different interfaces
  - Described in different languages
  - Different contracts, licenses (IP)
  - Different refinement levels
  - Different granularities
  - ➔ need a good system level model representing all these!

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Design methods & tools cnt'd

- How to hide low level circuit details and obtain RT performance?
  - High-level design metrics & performance estimation (active research)
- Two major tasks
  - Design space exploration
    - HW/SW partitioning
    - Selection of architecture
    - Selection of components
      - Reuse of predefined components
  - Architecture design
    - Design of components
    - HW/SW interface design

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HW architectures

- Philips Nexperia DVP (Now nxp.com)
  - Digital Video Platform
  - 1x VLIW media processor (32 or 64 bit, 100 - 300+MHz)
  - 1x MIPS core (32 or 64 bit, 50 – 300+ MHz)
  - library of dedicated HW processing units
- Texas Instruments (TI) OMAP Platform
  - for wireless applications
  - ARM9 core (150 MHz)
  - C55x DSP core (200 MHz)
  - dedicated memory and traffic controller
- Virtex-II Pro (Xilinx)
  - FPGA with 0,1,2 or 4 PowerPC cores
  - system bus, interfaces, HW IP's

All these platforms have severe limitations according to Jerraya & Wolf

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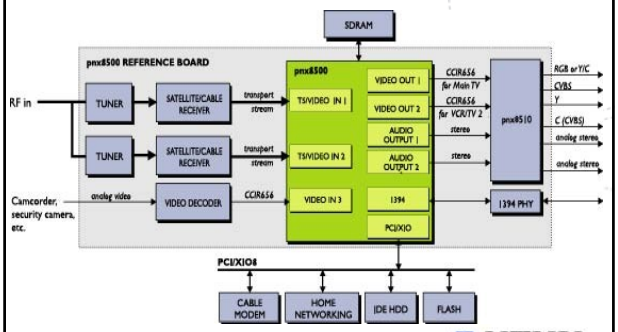
Philips Nexperia DVP



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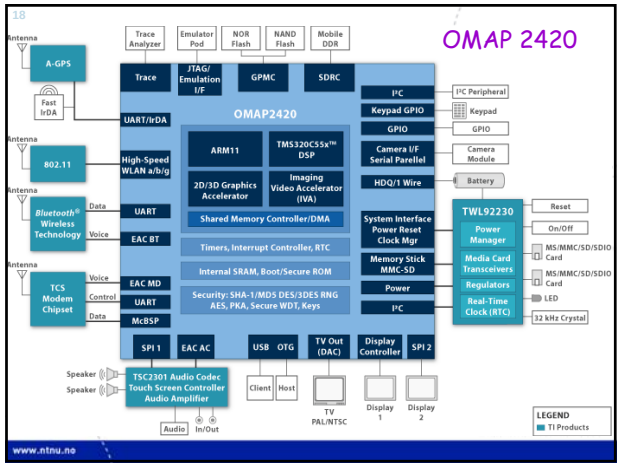

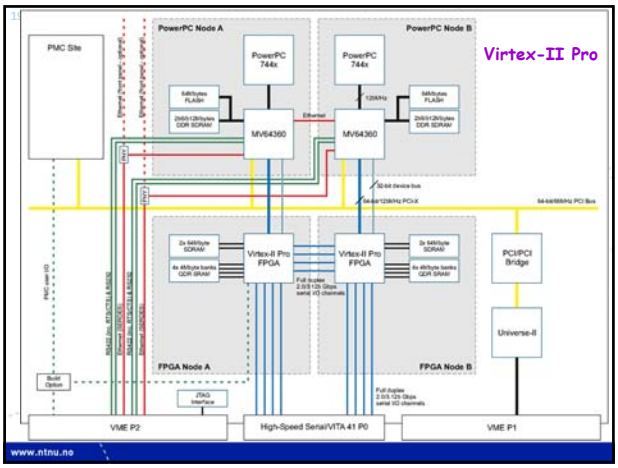

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MPSoC SW, programming

- Programming
  - parallel programming
    - shared memory (OpenMP, …)
    - message passing (MPI, …)
  - extra focus on efficiency
  - does not need all features in general parallel programming
  - heterogeneity makes programming worse
  - more massive parallelism (?)

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MPSoC SW, software architecture & design reuse

- Software architecture
  - Enables application SW to run on the MPSoC architecture
  - Provides a virtual machine
  - Abstraction and layering by application programming interfaces (APIs)
  - Contains
    - Middleware (communication)
      - between SW tasks
      - between SW and HW
    - Operating system (OS)
      - task scheduling
    - Hardware abstraction layer (HAL)
      - Context switch / bus drivers / config. code for MMU / interrupt handling
      - HAL-API is a contract between SW and HW designers ➔ HW & SW can be designed concurrently
  - Minimize overhead (limited time, area, power)
    - example: OS ➔ RTOS
- Well defined interfaces ➔ component reuse

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MPSoC software, optimization

- MPSoCs are often cost-sensitive RT-systems
- Software optimization
  - code size
  - execution time
  - energy consumption
- Processor architecture
  - parallelism, application-specific
  - configurable processor architecture
    - basic set of general instructions
    - application specific instructions can be added
    - example:Tensilica Xtensa
- Memory hierarchy (system)
  - shared memory
    - local cache & cache coherency
  - distributed memory
    - degree of distribution / granularity

"the only processor core for system-on-chip (SOC) designs that provides the I/O bandwidth, compute parallelism, and low-power optimization equivalent to hand-optimized, RTL-designed non-programmable hardware blocks. With Tensilica's unique XPRES Compiler and automated processor generator …"

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More design freedom – architecture important

- Most of the above-mentioned issues of processor architecture and memory hierarchy have been studied in the domains of processor architecture, compiler, and multiprocessor architecture. In the domain of MPSoC, researchers consider the **same problem in a different context with more design freedom in hardware architecture and with a new focus on energy consumption**.

  For instance, in the case of memory hierarchy design, conventional design methods assume that a set of regular structures are given. Application software code is then transformed to exploit the given memory hierarchy. However, **in the case of MPSoC, the designer can change the memory hierarchy in a way specific to the given application**. Thus, further optimization is possible with such hardware design freedom.

To what extent do we have the same design freedom for chip multiprocessor systems (CMP) ?

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References

- [HP03] Computer Architecture, A Quantitative Approach, 3rd ed., John Hennessy & David Patterson
- Much more reading
  - **MPSoC'07 presentations**
    - **http://www.mpsoc-forum.org/2007/index.html**

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