Defect Tolerant Ganged CMOS Minority Gate

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Abstract— **Production defects, resulting in faulty transistors, provide a challenge for the semiconductor industry in terms of reduced Yield. As defect densities are expected to increase as the semi-conductor feature size decreases, some form of transistor level defect tolerance is desirable to reduce this increasing production challenge. This paper proposes a solution, based on the ganged CMOS minority gate, for transistor level defect tolerance for minority gates.**

I. Introduction

As the semiconductor feature size decreases and the number of transistors on a single chip increases, one of the growing challenges facing the electronic design community is defective chips resulting in faulty behaviour [1].

There are several causes of defects, and defects may appear in different parts of an integrated circuit. This paper concentrates on transistor defects. A defective transistor may be modelled in several ways [2]. This paper considers stuck-open and stuck-closed defective transistors. A *stuck-open* transistor is a transistor that is never conducting, no matter what gate voltage is applied. A *stuck-closed* transistor is, on the other hand, always conducting.

The challenge of faulty transistors may be met by improved fault tolerance methods. Fault tolerance methods often involve the use of redundant hardware resources. Redundant hardware may be introduced at different levels. At the system level, one of the most popular redundancy techniques is *Triple Modular Redundancy* (TMR) [3]. Three equal modules calculate the same function and a voter outputs the majority output. TMR may also be applied at the gate level where each module is a smaller part of the complete system and where a cascade of TMR subsystems make up the complete system.

Defects may occur in any part of the system, including the voter. One disadvantage of TMR is the need for a perfect working voter or, if a perfect voter is not likely, triplicating the voter itself. The need for a voter makes TMR only practical when each of the modules are large compared to the voter. For TMR to function, the probability of having a functioning module must be more than 0.5. If the expected defect density of the IC is high, the modules must be small to ensure the probability of working is more than 0.5. If the defect density is high enough, TMR is no longer suitable because each module must be so small that the voter is dominating both in terms of area and susceptibility to defects.

A gate level alternative to TMR is *interwoven logic* [4] or *quadded logic* [5]. Quadded logic involves constructing the network of logic gates in a way such that it masks defects. Defect masking is achieved by quadrupling every gate in the system and connecting the gates in a specific way so as to avoid the need for a voter. The lack of a voter makes quadded logic useful at higher defect densities than TMR.

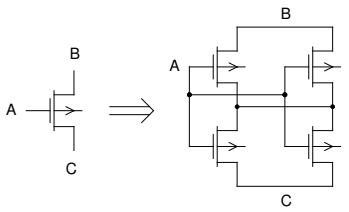

Fig. 1. Quadrupling transistors

When the expected defect density is so high that it is probable that a large amount of the digital gates are defective, gate level techniques like interwoven logic fail to mask all the defects. This makes it useful to introduce redundancy at the transistor level i.e. introducing redundant transistors when implementing the basic logic gates. Redundancy at the transistor level would help the systems reliability by providing robust gates. To get even higher reliability, these robust gates could be used together with gate level or system level redundancy techniques. Another benefit of introducing redundancy at the transistor level is to be able to exploit some non-digital properties of the transistor level architecture of the gate. These non-digital properties might lead to more efficient solutions areawise, than that what is possible at the Boolean gate level.

The focus of this paper is defect tolerance at the transistor level. More specifically, the focus is to make a three-input minority gate tolerant to all single stuck-open and stuck-closed defects.

Aunet and Hartmann [6] propose a solution where two or more identical minority gates drive the same output. Their solution is tolerant to stuck-open transistor faults. By requiring only twice the number of transistors, the method used by Aunet and Hartmann is an example of how the use of non-Boolean techniques may provide more efficient redundancy than what is possible at the Boolean gate level.

Anghel and Nicolaidis [7] propose a general transistor level defect tolerance method that handles both stuck-open and stuck-closed defects. This is achieved by quadrupling every transistor in the circuit, as shown in figure 1. By having two transistors in series, stuck-closed defects are tolerated. Two

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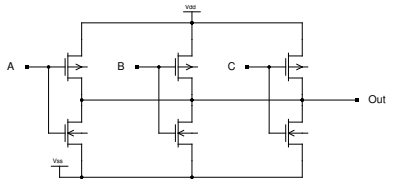


Fig. 2. Ganged CMOS minority gate implementation [8]

transistors in parallel tolerates stuck-open, much in the same way as in Aunet and Hartmann's work. Combining these as in figure 1 results in tolerance to both stuck-open and stuck-closed.

This paper starts in section II with a description and analysis of the ganged CMOS minority gate. The ganged CMOS minority gate is a specific minority gate implementation that is fundamental for the rest of the paper. Section III proposes a new minority gate implementation that is tolerant to all single stuck-open and stuck-closed transistors by building on the analysis in section II and previously known redundancy techniques. Section IV presents a simulation that compares different minority gate implementations with respect to reliability. A discussion of the properties of the proposed gate is given in section V and the paper concludes in section VI.

II. Ganged CMOS Minority Gate

The term ganged CMOS [9] refers to a CMOS circuit where the outputs of several inverters are wired together. Instead of acting as switches (standard digital CMOS), the transistors act as variable resistors controlled by their gate voltages. The circuit may thus be represented as a resistor network where conducting transistors are represented by small resistors and non-conducting transistors by large resistors [10]. Figure 2 illustrates a ganged CMOS minority gate, proposed in [11] as a majority gate (extra inverter at the output). Further, figure 3(a) presents the same circuit as a resistor circuit for the case where all inputs are zero.

Is it possible to exploit the concept of a resistor network for the minority gate so as to achieve defect tolerance? The approach taken in this section is to analyse what effect stuck-open faults could have on such a network and how these faults might be tolerated by sizing the transistors accordingly.

A. Characterisation of Minority Gate

The following analysis assumes three types of transistor behaviour: conducting (resistance r), non-conducting (resistance R) and stuck-open (resistance ∞), where R is much larger than r. Further it is assumed that only one pMOS transistor is stuck-open at a given time. The symmetric nature of the circuit implies that it is not necessary to check every combination of high inputs, but rather the four general cases: zero, one, two or three high inputs.

For each of the four cases, the ratio of the resistances of the pMOS and nMOS transistors is expressed. If a stuck-open transistor, represented as infinite resistance, provides a disadvantage to the pMOS/nMOS resistance ratio, the expressed ratio is adjusted to this worst-case scenario.

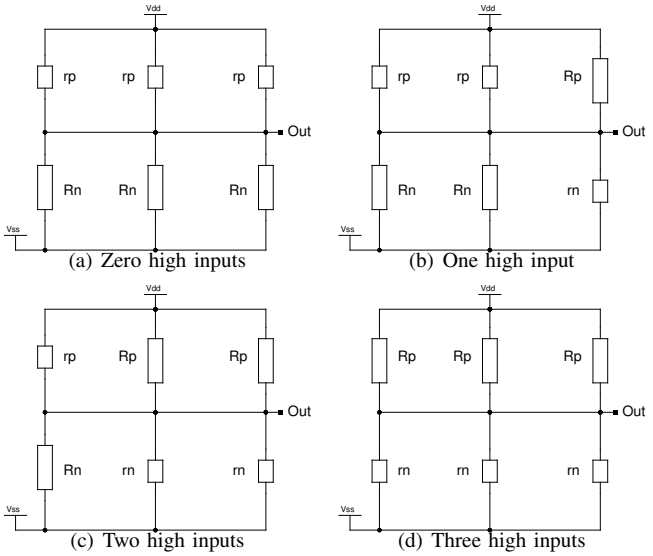


Fig. 3. Equivalent resistor network for gate in figure 2 for different inputs

Zero high inputs: When all inputs are zero, all pMOS transistors and no nMOS transistors conduct, resulting in the resistor network shown in figure 3(a) with an output close to V_{dd}. A stuck-open pMOS, represented as 0 in equation 1, provides a stricter condition (worst case) than that which directly represents the resistor network.

$$\left(0+\frac{1}{r_p}+\frac{1}{r_p}\right)^{-1} \ll \left(\frac{1}{R_n}+\frac{1}{R_n}+\frac{1}{R_n}\right)^{-1} \quad (1)$$

One high input: When one input is high, two pMOS and one nMOS are conducting, as illustrated in figure 3(b), and the output is close to V_{dd}. Similar to zero inputs, representing stuck open in equation (2) provides a worst case condition.

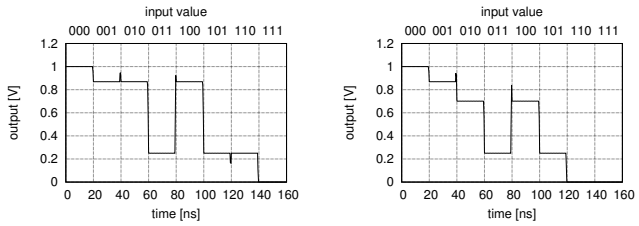
$$\left(0+\frac{1}{r_p}+\frac{1}{R_p}\right)^{-1} \ll \left(\frac{1}{R_n}+\frac{1}{R_n}+\frac{1}{r_n}\right)^{-1} \quad (2)$$

Two high inputs: As shown in figure 3(c), in this case, there is one conducting pMOS and two conducting nMOS transistors resulting in an output close to V_{ss}. Any stuck-open pMOS will increase the left hand side of the condition, thus positively affecting the condition. As such, a worst case condition is where no pMOS are stuck-open and thus equation (3) directly reflects the resistance network of figure 3(c).

$$\left(\frac{1}{r_p}+\frac{1}{R_p}+\frac{1}{R_p}\right)^{-1} \gg \left(\frac{1}{R_n}+\frac{1}{r_n}+\frac{1}{r_n}\right)^{-1} \quad (3)$$

Three high inputs: When all inputs are one, no pMOS and all nMOS transistors are conducting and the output is close to V_{ss}. When no pMOS transistors conduct then a stuck-open pMOS can only positively affect the output and is thus not reflected in equation (4).

$$\left(\frac{1}{R_p}+\frac{1}{R_p}+\frac{1}{R_p}\right)^{-1} \gg \left(\frac{1}{r_n}+\frac{1}{r_n}+\frac{1}{r_n}\right)^{-1} \quad (4)$$



(a) No faulty transistor (b) One pMOS stuck-open fault

Fig. 4. Simulation of gate in figure 2, showing gate output for all input combinations from 0 to 7. Inputs change every 20ns.

When condition (2) is satisfied, (1) is also satisfied because (2) is a tighter constraint. Likewise, if (3) is satisfied, (4) is also satisfied. In conclusion, this analysis suggests that when the conditions (2) and (3) are satisfied, the minority gate in figure 2 should have the correct output even when one of the pMOS transistors are stuck-open.

B. Case Study A

If transistors are sized properly, it is possible to satisfy conditions (2) and (3). To verify the above analysis and that the conditions are satisfied, a ganged CMOS minority gate was simulated. Ngspice [12] with the 22nm Berkeley Predictive Technology Models (BPTM) [13] and a supply voltage of 1V is employed as the simulator. Stuck-open transistors are modelled by removing the transistor from the SPICE netlist.

The transistor dimensions depend on the chosen technology. To find suitable transistor sizes for 22nm BPTM, a SPICE netlist representing conditions (2) and (3) were created and transistor sizes were manually adjusted until the conditions were satisfied. For this experiment, the following transistor dimensions were found suitable: $W_P = 90nm$, $L_P = W_N = L_N = 30nm$

Figure 4(a) shows a simulation of the minority gate when all transistors are working. All input combinations from 0 to 7 are shown, starting with input 0 at time 0 and changing input every 20ns. The output of the minority gate should be 11101000 (least significant bit first). Figure 4(a) show that the gate output is correct and differs from the ideal digital voltage with less then 0.25V. Figure 4(b) illustrates the operation of the minority gate in the presence of a stuck-open pMOS transistor. As can be seen, the output is still correct and less than 0.3V from the ideal output voltage. Symmetry ensures the same result for any stuck-open pMOS.

C. Limitations of Sizing for Defect Tolerance

To achieve tolerance to stuck-open nMOS transistors, a similar analysis and sizing adjustment is required. Studying the analysis of pMOS and nMOS defects at the same time provides conflicting conditions as shown in equation 5 (pMOS) and equation 6 (nMOS). As these conditions cannot both be fulfilled, no sizing adjustment will provide tolerance to both pMOS and nMOS stuck open defects. As such this technique is limited to tolerating single stuck-open defects in 50% of its transistors but requires no additional transistors.

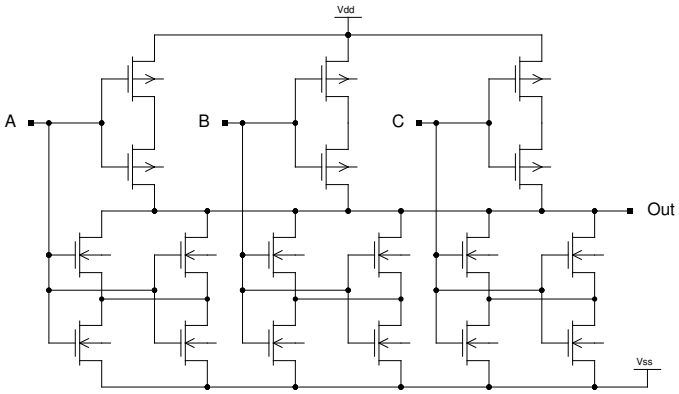


Fig. 5. New minority gate

$$\left(0 + \frac{1}{r_p} + \frac{1}{R_p}\right)^{-1} \ll \left(\frac{1}{R_n} + \frac{1}{R_n} + \frac{1}{r_n}\right)^{-1} \quad (5)$$

$$\left(\frac{1}{r_p} + \frac{1}{R_p} + \frac{1}{R_p}\right)^{-1} \gg \left(\frac{1}{R_n} + \frac{1}{r_n} + 0\right)^{-1} \quad (6)$$

III. Constructing a Defect Tolerant Minority Gate

To construct a minority gate tolerant to all single stuck-open and stuck-closed defects, the ganged CMOS minority gate and work in section II is used as basis. Each pMOS is sized, duplicated and placed in series so as to allow for both stuck-open and stuck-closed defects. To allow for both stuck-open and stuck-closed nMOS transistors, they are quadrupled in the same way as in Anghel and Nicolaidis [7], shown in figure 1. The resulting minority gate, tolerant to stuck-open and stuck-closed defects, is illustrated in figure 5.

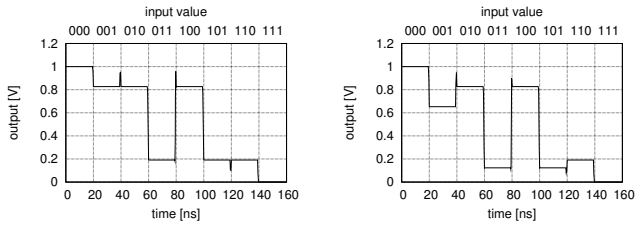
A. Case Study B

The same experimental setup is applied as in section II-B. Stuck-closed defects are simulated by substituting the faulty transistor with a 1Ω resistor between source and drain. Transistor dimensions are found manually, see section II-B. For the circuit in figure 5, the following transistor dimensions were found suitable: $W_P = 140nm$, $L_P = W_N = L_N = 30nm$.

Figure 6(a) shows simulated results with no faults applied. Figure 6(b) shows the same results with one stuck-closed nMOS. As seen, the output is correct in both cases. Only one of the possible defect configurations is shown. Simulations have shown that the output is correct with any single stuck-open or stuck-closed defective transistor. The gain is, however, dependent on the defect configuration, with defective pMOS transistors having the worst effect on gain.

IV. Comparing Reliability

The reliability R of a circuit is, in this paper, defined as the probability of having a correct output given a probability R_t that a transistor is functional. Further, it is assumed that each transistor fails independently with a certain probability



(a) No faulty transistor (b) One nMOS stuck-closed fault

Fig. 6. Simulation of gate in figure 5, showing gate output for all input combinations from 0 to 7. Inputs change every 20ns.

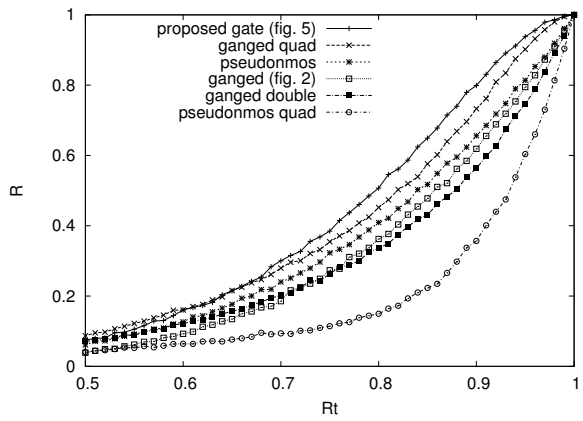


Fig. 7. Reliability of different minority gate implementations

$(1 - R_t)$. When failing, the transistor is either stuck-open or stuck-closed, each defect type being equally probable.

Monte Carlo simulations for different levels of transistor reliability R_t have been performed on the proposed minority gate of figure 5. For each R_t, 10000 different simulations are performed with random fault scenarios. The results have further been compared against similar simulations on five other minority gate implementations: the gate in figure 2 ("ganged"); a doubled version of figure 2 like in Aunet and Hartmann [6] ("ganged double"); a version of figure 2 quadrupled in a similar way as the circuits of Anghel and Nicolaidis [7] ("ganged quad"); a pseudo-nMOS minority gate ("pseudonmos"); and a quadrupled version of the pseudo-nMOS gate ("pseudonmos quad"). The results are presented in figure 7.

As can be seen from the Monte Carlo experiment, the new minority gate presented herein is more reliable than the other minority gate implementations for the given defect conditions. It is even better than "ganged quad". This can be explained by its smaller size (18 transistors for the proposed gate vs. 24 transistors for the quadrupled one). Fewer transistors in a gate means that the expected number of defective transistors is lower.

The redundant "ganged double" implementation is actually worse than the non-redundant "ganged" implementation. The doubling technique only tackles stuck-open defects and this experiment allow both stuck-open and stuck-closed. The larger size of "ganged double" compared to "ganged" makes it perform worse.

The non-redundant "pseudonmos" performs better than "ganged" because it uses only four transistors. It does however not benefit from quadrupling, as seen in the figure where "pseudonmos quad" has the lowest reliability of all the gates.

V. Discussion

As with other ganged CMOS implementations, this gate suffers from bad gain. Bad gain can be a problem if cascading several of these gates with no driver in between. A simple inverter on the output removes this problem and transforms the gate into a majority gate. If the inverter is quadrupled to make it defect tolerant, the resulting majority gate will have 26 transistors, still significantly smaller than the the 32 transistors needed for the fully quadrupled version.

VI. Conclusion and Further Work

This paper has analysed the ganged CMOS minority gate with respect to tolerance to defects. The analysis has provided conditions which, when met through transistor sizing, results in a circuit that exhibits tolerance to single stuck-open pMOS or nMOS defects. Further a revised ganged CMOS minority gate has been proposed with triple the transistor count but tolerant to both single stuck-open and stuck-closed faults. The results presented show that the proposed circuit is more reliable than the other ganged minority gate implementations it has been compared to, including the quadrupled implementation.

Further work will involve a study of how the proposed gate is affected by parameter variations. In addition, the Monte Carlo experiment should be repeated with other ways of modelling stuck-open and stuck-closed transistors as this might affect the reliability results.

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