Extreme Temperature Electronics - from Materials to Bio-inspired Adaptation

Dragana Laketic and Pauline C Haddow
Complex, Reconfigurable, Adaptive and Bio-inspired Hardware (CRAB) Lab
Department of Computer and Information Science
Norwegian University of Science and Technology
Email: (draganal,pauline)@idi.ntnu.no

Abstract

Biological systems have inherent mechanisms which ensure their adaptation and thus survival — preservation of functionality, despite extreme and varying environments. One such environmental feature is that of temperature. Extreme temperature electronics (ETE) is a field where, similarly, these organisms (electronic solutions), have to be designed to survive in such an environment. A number of approaches that address ETE are both proposed and, in some cases, implemented in today's technologies. Some of these approaches may be said to reduce this challenge but none may be said to solve it. However, biology has found a solution. There can, therefore, be great merit in turning to biology to identify possible solutions. However, it is important to first consider where the field is today.

This paper presents a survey of methods and techniques for tackling temperature effects in ETE — from materials to static and dynamic design techniques. Further, suggestions are provided as to where a bio-inspired approach may be applied either as an improvement to an existing approach or as a novel approach to an existing sub-challenge. Particular attention has been given to where a bio-inspired approach might provide a more dynamic solution.

1 Introduction

Electronic designs for the automotive, geothermal and petroleum deep-well drilling or space-craft industry all have one major challenge in common — they need to operate in extreme-temperature environments. This implies that Extreme Temperature Electronics (ETE) is required to operate in temperatures out with traditional commercial, industrial or military ranges i.e. out with $-55/-65\,^{\circ}\mathrm{C}$ to $+125\,^{\circ}\mathrm{C}$ [25]. The extremes of ETE are termed *high-temperature electronics* (HTE) referring to the temperatures over $+125\,^{\circ}\mathrm{C}$, *low-temperature electronics* (LTE) for the temperatures below $-55/-65\,^{\circ}\mathrm{C}$, and *cryogenic temperature electronics* i.e. below $-150\,^{\circ}\mathrm{C}$.

Living organisms are capable of survival despite dynamic and extreme environments. Finding ways to identify the fundamental mechanisms due to which such survival is achieved, may provide inspiration for ETE solutions not achievable by traditional methods. However, it is important to look at the existing traditional methods to identify where a bio-inspired approach might be advantageously combined with an existing approach or where such an approach alone might provide an improved solution or a novel solution to an unsolved problem. This paper presents a brief introduction to the challenges inherent in ETE, as well as a survey of ETE techniques and technologies under investigation. Moreover, it identifies avenues of research for bio-inspired techniques within ETE.

An overview of semiconductor properties and their variation under changing temperature conditions is provided in section 2. Existing approaches to ETE with fixed design solutions are surveyed in sections 3 and 4 — materials and design techniques respectively. Section 5 presents dynamic (adaptive) techniques and stresses the bio-inspired techniques as the promising guidelines for the novel solutions. Lastly, the conclusion remarks are given.

2 Theoretical background

Although new materials are under investigation and some materials are being applied to commercial devices, the majority of electronics today is based on semiconductor technology and, in particular, silicon. This section presents an overview of the challenges that silicon is facing with respect to extreme temperature environments and also different issues that need to be taken into account when considering semiconductors.

2.1 Operating point

The operation of an electronic device is described by its input-output characteristics. The operating point reflects the relationship between the inputs and outputs which describes the device functionality under given conditions. When exposed to extreme temperatures, this change in conditions causes the operating point to move resulting in a deviation in the device functionality.

2.2 Carrier mobility

Semiconductor materials are, in their native state, non-conducting materials. It is the ionised dopant atoms added to these materials that provide for the majority of electricity carriers in the material. However, the semiconductor intrinsic carriers can provide a certain amount of the total electricity carriers under specific conditions — see section 2.3.

Temperature variation causes an inverse exponential change in carrier mobility i.e. it is higher at low and lower at high temperatures. This kind of behaviour is a consequence of the fact that rising temperature makes atoms in the semiconductor crystal lattice vibrate causing more collisions with the dopant carriers — lattice scattering, making them less mobile [27].

2.3 Intrinsic carrier concentration

Rising temperature provides increased thermal energy to electrons in the semiconductor valence band. If this energy is higher than the semiconductor bandgap, the electron is promoted from the valence band to the conduction band thus contributing to a higher concentration of carriers and thereby increasing current. The concentration of intrinsic carriers is exponentially dependent on temperature. However, for the same temperature level and intrinsic carrier concentration, wider bandgap semiconductors exhibit lower current resulting from intrinsic electron promotion.

2.4 Threshold voltage

In CMOS technology, which is the dominating silicon technology today, threshold voltage shows linear dependence on temperature [34]. With technologies based on other materials, threshold voltage shows similar behaviour. It is only the parameters which determine its functional dependence on temperature that differ, for example the rate of the change.

2.5 Leakage current

Leakage current represents one of the challenges of silicon-based technology. In CMOS technology, there are several components which contribute to leakage current. Junction leakage, which is characteristic for reverse-biased p-n junctions, occurs at the junction between source or drain and the well due to minor carrier diffusion near the junction depletion region and also due to electron-hole pair generation within this region. Subthreshold leakage occurs when the gate voltage is below the threshold value. Further, there are also components caused by the gate electric field and other components which arise in short-channel devices [33]. Scaling towards nano-devices will increase leakage current effects.

2.6 Low-temperature behaviour

At very low temperatures MOS structures exhibit specific behaviour. Dopant carriers are frozen-out at specific low temperatures e.g. 30K for Si, where the thermal energy level is insufficient to ionise dopant atoms. This makes p-well and n-well perform similar to insulators [10]. As temperature lowers, the majority carriers are trapped at source making a bias at the well. The well bias causes threshold voltage to decrease which results in a current increase. For the particular value of the drain voltage the current saturates at a higher level than the Id-Vd characteristics. Thus the Id-Vd characteristic exhibits current kink and hysteresis at low temperatures. Other possible explanations for current kink may be seen in the literature [19, 48]. Current kink is more pronounced for n-MOS structure.

The freeze-out phenomenon in bipolar transistors is pronounced at base and collector sites. It affects the transistor frequency response, dynamic switching performance and the noise properties [9].

2.7 Zero-Temperature-Coefficient (ZTC) bias points

ZTC bias points refer to the two gate bias voltage points, one in linear another in the saturation region of the MOSFET structure, for which drain current is least affected by temperature [34]. This phenomenon can be exploited for tackling the temperature effects in MOSFETs through biasing schemes, see [14].

2.8 Semiconductor Crystal Structure

All semiconductor substrate wafers have single-crystal structures. Such a structure exhibits higher periodicity, making the dopant movement through the crystal structure easier. Therefore, the quality of the crystal structure greatly influences semiconducting properties such as carrier mobility. On the other hand, all semiconductor dielectrics are amorphous. The amorphous nature of the structure prevents electricity movement yielding material dielectric properties [22].

Single-crystal structures are, therefore, sought for future electronics based on synthetic semi-conducting materials. These materials are generated through the process of epitaxial i.e. layer-by-layer growth during which impurities are added. However, for many potential materials it is very hard to achieve a defect-free single-crystal structure during this process.

2.9 Packaging and Wiring

Operation of the electronic device at extreme temperatures is limited not only by the temperature-induced phenomena and temperature-dependent properties of its components, but also by the packaging and wiring. At high temperatures the interaction between materials is more pronounced due to the presence of higher thermal energy.

A number of aspects need to be addressed: characterisation of materials and their interactions at high temperatures; minimisation of mechanical stresses caused by thermal expansion mismatches; provision of heat dissipation path and environmental protection; improvements in metallisation and device development tools and testing equipment [28].

3 New Materials for Extreme Temperatures

One approach to tackling temperature effects is to exploit the fact that materials behave differently at varying temperatures according to their intrinsic properties. In general, materials for extreme temperatures may be classed into those addressing high temperature issues and those addressing low temperature issues.

3.1 High Temperature Semiconductor Materials

One of the most important semiconductor properties for high temperature operation, is the bandgap width. Wide bandgap semiconductors require more thermal energy to excite electrons from the valence band.

Another property of interest for high temperatures is intrinsic carrier concentration. The current component caused by the increase of intrinsic carriers in the conduction band at higher temperatures will be lower if the concentration is lower.

Various wide bandgap semiconductors have already been tested for ETE: SiC, Diamond, GaAs, nitrides and their alloys. Their suitability for ETE devices depends on production advances, especially with respect to achieving defect-free single-crystal semiconductor structures that can easily be doped. However, recently reported results on the epitaxial growth processes for SiC and Diamond are very promising [45] and terms like *SiC electronics* or *diamond electronics* have become common phrases in the ETE community. Some selected properties of these materials, as well as silicon itself, are provided in table 1.

Table 1. Physical Properties for Some Semiconductor Materials, [45], [21]

Name	Bandgap (eV)	Carrier mobility, μ (cm^2/Vs)	Intrinsic carrier concentration (cm^{-3})
Si	1.1	1350el 480holes	$1.02 \cdot 10^{10}$
GaAs	1.4	8600el 250holes	$2.1 \cdot 10^{6}$
SiC	3.3	980el 200holes	$3 \cdot 10^{15}$ (3C-SiC)
GaN	3.4	2000el 200holes	$1.9 \cdot 10^{-10}$
Diamond(C)	5.5	3500-4500el 2600-3800holes	$1 \cdot 10^{-27}$
Ge	0.66	3900el 1900holes	$2 \cdot 10^{13}$

GaAs behaves as silicon at extreme temperatures, exhibiting the same kind of temperature effects. It is the diffusion component of the leakage current that becomes significant at higher temperatures than in Si [35] due to its wider bandgap, see table 1. GaN, on the other hand, is characterised by high carrier mobility. Together with other compounds from the same family of nitrides: InN; AlN and their alloys, GaN has demonstrated operation at temperatures as high as $500\,^{\circ}\mathrm{C}$ [11]. SiC is characterised by very low intrinsic carrier concentrations resulting in current increases at higher temperatures. Devices based on SiC have demonstrated operation at temperatures above $400\,^{\circ}\mathrm{C}$, [46].

Diamond is the most promising material of all, not only because of the widest bandgap, but also the highest thermal conductivity amongst all solids. Further, diamond exhibits strong mechanical properties and resistance to high-energy radiation. However, the current state of research into diamond-based electronics is focused on synthetic diamond wafer production.

Some technologies employ other materials in combination with traditional semiconducting materials in order to reduce undesirable temperature effects e.g. semiconductor-on-insulator structures [47]. These structures have a layer of insulator between the MOS body and the wafer substrate which reduces leakage current effects.

Germanium has not proved to be suitable for higher temperature applications due to its narrow bandgap, see Table 1. However, recent results [7] and [8] show that SiGe heterojunction bipolar transistors (HBT) can be used for higher temperatures of up to 300 °C. The description of high temperature behaviour of SiGe heterostructures may be found in [12].

3.2 Low Temperature Semiconductor Materials

The materials that are currently under investigation for low temperatures include Ge, GaAs and Si. During material production, special process parameters such as epitaxial layer thickness and doping concentration are applied in order to yield devices fit to operate at low temperatures.

Various devices based on Ge have been demonstrated to maintain satisfactory operational characteristics at low temperatures. These devices include: Ge-based diode; bipolar transistor and a metal-insulator-semiconductor capacitor (MIS) [42]. A Ge JFET was demonstrated to operate with stable DC characteristics and low gate reverse leakage current at temperatures as low as 4K. However, noise was a problem at this low temperature although the device tolerated noise as low as 20K [44]. GeSi hetero-structures compatible with existing silicon technologies are also suitable for low temperatures [3], [12].

3.3 Materials discussion

As the new generation of semiconductors is emerging [45], there are many questions raised which need to be answered before devices based on the new materials reach the stage of mass production. Are the devices expected to follow ASIC design i.e. fixed during the production process or is there a possibility for reconfigurable devices? Will the design of these devices follow the same rules as those applied to the design of silicon devices? If not, can current design methods be adapted to the new devices or are novel design methods required? Could the novel design for the devices based on new materials seek inspiration from biological patterns? Some of the technological difficulties met in their production might be solved by turning to the biological ways of constructing tissue.

4 Design Techniques for ETE

Temperature effects can be tackled by building compensation schemes into the circuit or system design. These compensation schemes refer to circuitry which is added to a design to compensate for temperature-caused phenomena.

4.1 Compensation Design Techniques

For leakage current compensation, conventional methods consist of building-in compensation diodes whose inversion current compensates for the unwanted MOSFET's leakage current, following Kirchoffs law. Instead of diodes, current mirrors can be introduced [26].

Compensation schemes for operational amplifiers (OpAmps) have drawn a lot of attention because of their important role in analogue circuits. Each stage has different schemes depending on their specificities. The input stage compensation is similar to MOSFET compensation. Various schemes are proposed for further improvements such as in [40]. For the compensation of middle gain stages, supply voltage division schemes are applied [34] where compensation depends on the ratio of passive elements in the compensation circuitry. The output stage does not need any additional circuitry as n-MOS and p-MOS leakage currents have opposite directions. However, the leakage areas in these output stage transistors are required to be equal for these currents to compensate one other [34].

Another approach to OpAmp compensation at extreme-temperatures is auto-zeroing. Auto-zeroing is a method applied in OpAmps for the voltage offset cancellation. There are different ways in which it can be realised. One example with offset current compensation is presented in [20], another which includes pre-amplifiers in [40].

AD converters are another group of devices which are important for ETE applications. There are various design techniques applied for their compensation. The switched bridge topology, presented in [20], performs error suppression at high temperatures. AD converters which require matching of less temperature-dependent passive components, such as capacitors, are more suitable for extreme temperatures than those based on temperature-dependent resistors. Examples of such AD converters include pipeline and sigma-delta [40].

4.2 Technological Design Techniques

Technological design can also account for lowering extreme temperature effects. Current kink, which MOS transistors exhibit at cryogenic temperatures, can be eliminated by floating the well, see [15] [23]. Graded channels in SOI MOSFETs [29] as well as double-gate design [30] are also suitable design techniques for low temperatures.

Another example is SiGe HBT where the shape of the Ge profile near the emitter-base junction influences the magnitude of the current gain. For the suitable Ge profile, the current gain can even become temperature independent [9].

4.3 Design Discussion

All compensation techniques, no matter how well designed or how well the technological properties are adjusted, still face certain temperature limits after which operation is temperature-degraded. Can these techniques be modified in order to preserve their compensating role even when this limit is surpassed? What mechanism could guide the modification? Could some novel, bio-inspired solution yield the modification in the design which would preserve its compensating role irrespective of the existing temperature limits? The principles underlying thermoregulatory mechanisms in the human body could be used as a source of inspiration.

5 Adaptation to Extreme Temperatures

Traditional approaches to adaptive solutions presume that changed conditions, to which the device is going to be exposed, are well-specified during the design phase. Different solutions may be created for these specific conditions, all of which are available at run-time and applied as the temperature conditions are changed. This means that a device may switch between those predefined solutions instead of one static solution (as in sections 3 and 4). However, even if different temperatures are known in advance and the suitable design solutions created, there is still an open question: how should the design be switched in real-time?

Depending on the application in hand, it is not always possible to specify the temperature conditions at design time. To adapt to changing temperature conditions at run-time involves the creating a new design solution tailored to the changing conditions. One possible run-time adaptive solution is to apply an evolutionary algorithm to search for the new solution, as described in section 5.1.

5.1 Self-Reconfigurable Electronics for Extreme Environments (SRE-EE)

At NASAs Jet Propulsion Laboratory (JPL), a generic platform for achieving designs adaptable to extreme environments: Self-Reconfigurable Electronics for Extreme Environments (SRE-EE), is being developed. Further, various functional designs have been implemented and tested for extreme temperature tolerance.

The platform consists, in principle, of a number of programmable elements interconnected by programmable switches that may be switched on/off under the control of an evolutionary algorithm — a bio-inspired algorithm inspired by natural evolution. Depending on the state of the switches, different circuit topologies can be obtained thus resulting in different functionalities. The first version consisted only of programmable transistors, whilst later versions contain additional elements: capacitors, resistances, amplifiers and even arrays of sensors.

The main temperature-dependent characteristic of silicon that is being addressed is that of the operating point. The goal being to adapt the operating point in an extreme temperature environment such that the original functionality may be recovered or new functionality may be achieved.

Applications that were tested varied from logic gates, a Gaussian-shaped curve, a half-wave rectifier, closed-loop OpAmps, different types of filters and controllable oscillators. In more recent experiments [37, 39] it was not only the circuit itself which was exposed to extreme temperatures, but also the evolutionary algorithm controlling the adaptation. The functions were tested in various experimental setups to either high or low temperatures. The results of the experiments are very promising, especially in the light of the exposure of the evolutionary algorithm itself, ensuring that the experiment could be repeated at these extreme temperatures in a less accessible environment.

It is interesting to note that in some cases functionality was recovered when the design was implemented in an older platform version i.e. produced in 0.5μ CMOS, whilst the design failed to recover when implemented on a platform produced in a newer technology 0.18μ CMOS, [49]. It shows that scaling of transistors increases the temperature challenge, as stated in section 2.

Further, the possibility of exploiting extreme temperatures to achieve new functionality was investigated. Preliminary results showed that a design performing logical AND at one temperature could achieve a logical OR at another [38]. These types of circuits, where functionality can be controlled by some parameter including temperature, power supply or voltage have been termed *polymorphic electronics*. However, the work in this area is at a very early stage.

5.2 Bio-inspired Adaptation

Many human biological processes may be characterised as adaptive to changing environments e.g. the immune system and endocrine system. Such systems have been investigated, not particularly for ETE, but rather for fault recovery in digital systems [5] and [16].

A further interesting biological process is homeostasis: when an organism is exposed to a stressful situation, excessive light or temperature, it triggers a chain of reactions which preserve the organism's balance. In this process, physiological and bio-chemical actions and reactions happen at different levels — from the organism as a whole down to the processes within a cell. The result of these processes is that the organism survives despite environmental changes — a feature desirable in ETE applications. Further, biological tissues and their composition provide reconfigurable structures which are adaptable to environmental changes. Homeostasis is preserved thanks to the interplay of many mechanisms which include all organs and tissues of the body performing their functions [17].

A homeostasis inspired approach to ETE might similarly be applied at different levels, from the design as a whole down to subsystems of the design. A part of the system might be adapted to the new conditions - similar to the work at 5.1 or the part might be replaced by another part which can take voter and provide the overall desirable operation under the new conditions. The latter scenario may be seen as similar to that of a cell in a living organism — it is replaced by another cell when it is no longer capable of performing its intended function.

6 Conclusion Remarks and Future Work

Extreme-temperature electronics is a broad field in which a number of challenges have been addressed but not solved. The survey of the field provided in this paper has presented materials and conventional methods, as well as bio-inspired techniques designed to tackle the effects caused by ETE. Some questions with respect to these approaches have been raised and directions for novel solutions suggested.

Biological processes, in the form of thermoregulatory mechanisms, involving different organs, tissues and cells offer inspiration for novel ETE approaches. Future work will investigate such processes in the light of real-time adaptive ETE solutions.

References

[1] A. Aleksov, M. Kubovic, N. Kaeb, U. Spitzberg, A. Bergmaier, G. Dollinger, T. Bauer, M. Schreck, B. Stritzker, and E. Kohn. Diamond field effect transistors - concepts and challenges. In *Diamond and Related Materials 12*, pages 391–398. Elsevier Science, 2003.

[2] G. Amaratunga. A dawn for carbon electronics? In *Science, Vol. 297*, pages 1657–1658, September 2002.

[3] F. Aniel, M. Enciso-Aguilar, N. Zerounian, L. Giguerre, P. Crozat, R. Adde, M. Zeuner, G. Hock, T. Hackbarth, H. Herzog, and U. Konig. Sige hetero fets on silicon at cryogenic temperature. In *Journal de Physique IV*, pages 3–10, 2002.

[4] J. Batista, A. Mandelis, and D. Shaughnessy. Temperature dependence of carrier mobility in si wafers measured by infrared photocarrier radiometry. In *Applied Physics Letters, Vol. 82, No. 23*, pages 4077–4079, June 2003.

[5] D. Bradley and A. Tyrrell. Immunotronics: Hardware fault tolerance inspired by the immune system. In *LNCS, Evolvable Systems: From Biology to Hardware: Third International Conference, ICES*, pages 11–20, April 2000.

[6] M. Chan, P. Su, H. Wan, C. Lin, S. Fung, A. Niknejad, C. Hu, and P. Ko. Modeling the floating-body effects of fully depleted, partially depleted, and body-grounded soi mosfets. In *Solid-State Electronics 48*, pages 969–978, 2004.

[7] T. Chen. Operation of sige bicmos technology under extreme environments. In *Thesis for the Degree of Doctor of Phylosophy*. Georgia Institute of Technology, School of Electrical and Computr Engineering, December 2005.

[8] T. Chen, W. L. Kuo, E. Zhao, Q. Liang, Z. Jin, J. Cressler, and A. Joseph. On the high-temperature (to 300 c) characteristics of sige hbts. In *IEEE Transactions on Electron Devices, Vol. 51, No. 11*, pages 1825–1832, November 2004.

[9] J. Cressler and G. Niu. Temperature effects. In *Silicon-Germanium Heterojunction Bipolar Transistor*. Artech House, Inc, 2003.

[10] B. Dierickx, L. Warmerdam, E. Simoen, J. Vermeiren, and C. Claeys. Model for hysteresis and kink behavior of mos transistors operating at 4.2 k. In *IEEE Transactions on Electron Devices, vol.35, no.7*, pages 1120–1125, July 1988.

[11] J. Edgar, S. Strite, I. Akasaki, H. Amano, and C. Wetzel. Properties, processing and applications of gallium nitride and related semiconductors. In *The Institution of Electrical Engineers*, 1999.

[12] J. D. C. (Editor). Temperature effects. In *Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy*. Taylor & Francis Group, CRC Press, 2006.

[13] C. Enz and G.C.Temes. Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization. In *IEEE , Proceedings*, pages 1584–1614, November 1996.

[14] I. Filanovsky and A. Allam. Mutual compensation of mobility and threshold voltage temperature effects with applications in cmos circuits. In *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol.48, No.7*, July 2001.

[15] G.Oleszek. Carrier freeze-out and relaxation effects in cmos n-channel mosfets at cryogenic temperatures under dynamic operating conditions. In *Sixth International Symposium on Low Temperature Electronics*, September 2001.

[16] A. Greensted and A. Tyrrell. Fault tolerance via endocrinologic based communication for multiprocessor systems. In *LNCS, Evolvable Systems: From Biology to Hardware: Fifth International Conference, ICES*, pages 24–34, March 2003.

[17] A. Guyton and J. Hall. Functional organization of the human body and control of the internal environment. In *Textbook of Medical Physiology*. Elsevier Saunders, 2006.

[18] A. Hairapetian, D. Gitlin, and C. Viswanathan. Low-temperature mobility measurements on cmos devices. In *IEEE Transactions on Electron Devices, VOl. 36. No.8*, pages 1448–1455, 1989.

[19] H. Hanamura, M. Aoki, T. Masuhara, O. Minato, Y. Sakai, and T. Hayashida. Operation of bulk cmos devices at very low temperatures. In *IEEE Journal of Solid-State Circuits*, pages 484– 490, June 1986.

[20] J. Haslett, F. Trofimenkoff, I. Finvers, F. Sabouri, and R. Smallwood. High temperature electronics using silicon technology. In *IEEE International Solid-State Circuits Conference, Proceedings*, February 1996.

[21] J.Isberg, J. Hammersberg, E. Johansson, T. Wikstrom, D. Twitchen, A. Whitehead, S. Coe, and G. Scarsbrook.

High carrier mobility in single-crystal plasma-deposited diamond. In *Science, Vol. 297*, pages 1670–1672, September 2002.

[22] J.Ruzyllo. Crystal structure. In *Semiconductor OneSource: Semiconductor Note 13*, August 2005.

[23] K. Kasley, G. Oleszek, and R. Anderson. Impact of floating the well contact on the low temperature kink in n-channel cmos transistors. In *Proceedings of the Workshop on Low Temperature Semiconductor Electronics*, pages 128–132, August 1989.

[24] D. Keymeulen, R. Zebulum, R. Rajeshuni, A. Stoica, S. Katkoori, S. Graves, F. Novak, and C. Antill. Self-adaptive system based on field programmable gate array for extreme temperature electronics. In *Proceedings of the First NASA/ESA Conference on Adaptive Hardware and Systems*. NASA/ESA, July 2006.

[25] R. Kirschman. Extreme-temperature electronics, tutorial. In *On Extreme-Temperature Electronics by R. Kirschman*, December 2006.

[26] K. Mizuno, N. Ohta, F. Kitagawa, and H. Nagase. Analog cmos integrated circuits for high-temperature operation with leakage current compensation. In *Fourth International High Temperature Electronics Conference*, June 1998.

[27] P. Neudeck, R. Okojie, and L. Chen. High-temperature electronics - a role for wide bandgap semiconductors? In *Proceedings of the IEEE, Vol. 94, No. 12*, pages 1065– 1076, June 2002.

[28] C. on Materials for High-Temperature Semiconductor Devices. National materials advisory board, commission on engineering and technical systems, national research council. In *Materials for High-Temperature Semiconductor Devices*. National Academy Press, Washington D.C., 1995.

[29] M. Pavanello, P. D. Agopian, J. Martino, and D. Flandre. Low temperature operation of graded-channel soi nmosfets for analog applications. In *Journal de Physique IV*, pages 23–26, 2002.

[30] M. Pavanello, J. Martino, T. Chung, A. Kranti, J. Raskin, and D. Flandre. Operation of double gate graded-channel transistors at low temperatures. In *The Electrochemical Society, Inc., 204th Meeting*, October 2003.

[31] P.G.Neudeck. Progress towards high temperature, high power sic devices. In *International Symposium on Compound Semiconductors, San Diego*, September 1994.

[32] M. Pratapgarhwala. Temperature mismatch effects, chapter iv. In *Characterization of Transistor Matching in Silion-Germanium Heterojunction Bipolar Transistors, Master Thesis*, pages 34–41. Georgia Institute of Technology, School of Electrical and Computr Engineering, December 2005.

[33] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand. Leakage current mechanisms and leakage reduction techniques in deep-submicrometer cmos circuits. In *Proceedings of the IEEE, Vol. 91, No. 2*, pages 305–327, February 2003.

[34] F. Shoucair. Design considerations in high temperature analog cmos integrated circuits. In *IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-9, No.3*, pages 242–251, 1986.

[35] F. Shoucair and P. Ojala. High-temperature electrical characteristics of gaas mesfet's (25-400 c). In *IEEE Transactions on Electron Devices, VOl. 39. No.7*, pages 1551–1557, 1992.

[36] S.T.Lee and Y. Lifshitz. The road to diamond wafers. In *Nature, Vol.424*, pages 500–501, July 2003.

[37] A. Stoica, V. Lacayo, R. Rajeshuni, D. Keymeulen, R. Zebulum, J. Neff, G. Burke, and T. Daud. Re-configurable electronics behavior under extreme thermal environment. In *MAPLD International COnference*, September 2005.

[38] A. Stoica, R. Zebulum, and D. Keymeulen. Polymorphic electronics. In *International Conference on Evolvable Systems*, October 2001.

[39] A. Stoica, R. Zebulum, D. Keymeulen, R. Ramesham, J. Neff, and S. Katkoori. Temperature-adaptive circuits on reconfigurable analog arrays. In *Proceedings of the First NASA/ESA Conference on Adaptive Hardware and Systems*. NASA/ESA, July 2006.

[40] S. Terry, B. Blalock, J. Jackson, S. Chen, C. Durisety, M.M.Mojarradi, and E. Kolawa. Development of robust analog and mixed-signal electronics for extreme environment applications. In *IEEE Aerospace COnference, Proceedings*, March 2004.

[41] A. Vassighi and M. Sachdev. Low temperature cmos operation. In *Thermal and Power Management of Integrated Circuits*. Springer US, 2003.

[42] R. Ward, W. Dawson, R. Kirschman, O. Mueller, R. Patterson, J. Dickman, and A. Hammoud. Ge semiconductor devices for cryogenic power electronics - ii. In *Journal de Physique IV*, 2002.

[43] R. Ward, R. Kirschman, M. Jhabvala, R. Babu, D. Camin, and V. Grassi. Development of ge jfets for deep-cryogenic preamplifiers. In *Proceedings of SPIE, Vol. 4850, IR Space Telescopes and Instruments*, pages 910–918, March 2003.

[44] R. Ward, R. Kirschman, M. Jhabvala, R. Babu, N. Das, D. Camin, V. Grassi, K. Kandiah, and J. Rosenberg. Development of cryogenic ge jfets - iii. In *Fourth European Workshop on Low Temperature Electronics*, June 2000.

[45] M. Willander, M. Friesel, Q. Wahab, and B. Straumal. Silicon carbide and diamond for high temperature device applications. In *Journal of Materials Science: Materials in Electronics 17*, pages 1–25, 2006.

[46] W. Wondrak, E. Niemann, R. Held, R. Constapel, and G. Kroetz. Sic devices for power and high-temperature applications. In *IEEE*, pages 153–156, 1998.

[47] U. V. Ya. Novel soi mosfet structure for operation over a wide range of temperatures. In *Science and Technology of Semiconductor-On-Insulator Structures and Devices Operating in a Harsh Environment*, pages 179–184. Kluwer Academic Publishers, 2005.

[48] H. Zappe, R. Gupta, I. Sakai, and C. Hu. Operation of cmos devices with a floating well. In *IEEE Transactions on Electronic Devices, Vol. 34, No. 2*, pages 335–343, February 1987.

[49] R. Zebulum, D. Keymeulen, V. Duong, X. Guo, M. Ferguson, and A. Stoica. High temperature experiments using programmable transistor array. In *Aerospace Conference, Proceedings*, March 2004.