The Wire-speed processor
So... what is this thing?

- It’s a heterogeneous processor architecture
  - Generic cores
  - Domain-specific accelerators
- Accelerators with **uniform** interfaces
  - Increased performance
  - Simpler programming model
So... what is this thing?

- It’s a processor: “the WSP”
  - Large number of moderate-performance and low-power cores
  - Targeted toward network applications
WSP architecture

Optimized for parallel processing: large pool of threads and superior performance per watt. Optimized accelerators and packet processor interface.

Four A2 cores
L2 cache

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L2 cache

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L2 cache

Four A2 cores
L2 cache

MemCtrl

MemCtrl

XML
Regex
Comp
Crypto

Full set of accelerators for processing-intensive functions

OS bypass: accelerators and packet processor operate in application virtual space

External PBUS interface

High-speed interconnect accelerator and packet processor cache inject

PCle - gen2

Packet processing engine

4 x 10 Gigabit Ethernet MAC

Centralized media speed functions: packet classification, core/thread selection and scheduling, packet ordering, traffic management QoS, and integrated network interface.
Interconnect complex, “PBus”

- Connects internal and external components together
- Provides cache coherency and data protocol
- Designed to scale
- Each unit implements a customised PBus interface controller
Processor complex

- 16 PowerPC A2 cores
- 2.3 GHz
- Four simultaneous threads of execution per core
- Implements standard Power ISA
Processor complex, low-power wait res

- Accelerators introduce high level of asynchronicity
- Load and Reserve
  - reserves a cache-line
- waitrsrv
  - The thread sleeps until reservation of cache-line is lost
Accelerator complex

- Can incorporate devices such as GPUs, FPGAs, other cores from any ISA
- icswx
  - creates a cache-aligned coprocessor request block (CRB)
  - Available to all privilege levels
- ACOP register (available coprocessor)
  - Per-Thread register
  - Restrict access of an application to particular accelerators
Accelerator complex, CRB

- Machine Status Bits describes an application’s privileges
- Each accelerator have a CT and CI together forming a unique identifier
  - Coprocessor Type: Unique for every type
  - Coprocessor instance: Unique for every instance within a “type”-group
- Status and completion block defines how the core should be notified on completion
Accelerator complex, bus interface

- Accelerator complex separated into generic bus interface and accelerator units
  - Simplifies accelerator design
- Bus interface are responsible for
  - Snoop the bus for CRBs
  - Provide validation
  - Queue requests
  - Facilitate buffered memory access
  - Provide address translation
Accelerators in WSP

- Six hardware accelerators
  - Cryptographic
  - Compression/decompression
  - Pattern matching
  - XML
  - Ethernet packet processing
  - PCIe DMA engine
- Several accelerators provide multiple engines which allows for parallel work
- Runtime environment provides accelerated versions of standard libraries (OpenSSL, libz...)
Network I/O complex

- WSP relies on massive parallel processing when performing network processing in software
- Inherently serial computation is hardware accelerated.
Summary

- Heterogeneous architecture
- Improved accelerator programming model
- Accelerators and processors living together as first-class-citizens
- Questions?